Notes from Calhoun on our Conference Paper:

* Low power 1Mb SRAM. Design emphasis on optimizing block sizes and aspect ratios using a parameterized model of the memory macro. Also optimized VDD separately for active and idle modes.
* Bitcell: opted for min sized devices. Although this gave positive margins at no variation, the paper doesn’t justify that they are sufficiently high (gives 78mV as margin at 600mV VDD). Given that the group took the extra step to account for variability in other parts of the design, it’s unfortunate that they didn’t do so in the bitcell sizing. Used M-C sim to find minimum VDD during standby – selected a VDD that gives no errors below 10% of VDD, although this is for a 1k point sim. No discussion of yield for the 1Mb array.
* Array Model: Uses only 4 active bitcells – probably better to use a 32b word. Very nice presentation of results from the model showing the tradeoffs with array partitioning. Could have shown the breakdown of power at different points to illustrate why these results  exhibit the trends that they do.
* Metric: Good description of the final metric computation. Delay accounts for worst case corners.
* Not clear from the paper what the final status of layout was.
* Overall, this was a very strong project. I find the results quite believable and am pleased with the robust correct operation of this memory.